

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (withdrawn): A method of forming a semiconductor varactor, comprising:
forming a well region of a first conductivity type in a semiconductor substrate;
forming a gate dielectric layer on said well region;
forming a gate layer on said gate dielectric layer;
forming contact regions in said well region of a first conductivity type; and
forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie said well region.

Claim 2 (withdrawn): The method of claim 1 further comprising forming sidewall structures adjacent to said gate layer.

Claim 3 (withdrawn): The method of claim 2 wherein said well region is n-type.

Claim 4 (withdrawn): The method of claim 2 wherein said well region is p-type.

Claim 5 (withdrawn): The method of claim 1 wherein said forming gate layer contacts comprises forming said gate layer contacts to said gate layer over an active area of said semiconductor varactor.

Claim 6 (withdrawn): A semiconductor varactor, comprising:

a well region of a first conductivity type in a semiconductor substrate;
a gate dielectric layer on said well region;
a gate layer on said gate dielectric layer;
contact regions in said well region of a first conductivity type; and
gate layer contacts to said gate layer wherein said gate contacts overlie said well region.

Claim 7 (withdrawn): The semiconductor varactor of claim 6 further comprising sidewall structures adjacent to said gate layer.

Claim 8 (withdrawn): The semiconductor varactor of claim 7 wherein said well region is n-type.

Claim 9 (withdrawn): The semiconductor varactor of claim 7 wherein said well region is p-type.

Claim 10 (withdrawn): The semiconductor varactor of claim 6 wherein said gate layer contacts comprises gate layer contacts to said gate layer over an active region of said semiconductor varactor.

Claim 11 (currently amended): A method for forming a low resistance semiconductor

varactor, comprising

providing a semiconductor substrate with at least a first isolation region and a second isolation region separated by a first distance;

forming a well region of a first conductivity type in said semiconductor substrate between said first isolation region and said second isolation region;

forming at least a first and second active regions in said well region by forming a contact isolation structure in said well region between said first isolation region and said second isolation region;

forming contact regions on a first conductivity type in said first and second active regions;

forming a gate dielectric layer on said first active region and said second active region;

forming a gate layer on said gate dielectric layer wherein said gate layer overlies said first active region, said second active region, and said contact isolation region; and

forming electrical contacts to said gate conductive layer wherein said electrical contacts are formed over said contact isolation region.

Claim 12 (original): The method of claim 11 wherein said first and second isolation regions comprise STI structures.

Claim 13 (original): The method of claim 11 wherein said contact isolation structure comprises a STI structure.

Claim 14 (original): The method of claim 11 further comprising forming well contact regions adjacent to said first and second isolation regions.

Claim 15 (withdrawn): A low resistance semiconductor varactor, comprising providing a semiconductor substrate with at least a first isolation region and a second isolation region separated by a first distance; a well region in said semiconductor substrate between said first isolation region and said second isolation region; a contact isolation structure in said well region between said first isolation region and said second isolation region; a gate dielectric layer on said well region and said contact isolation region; a gate layer on said gate dielectric layer wherein said gate layer overlies said contact isolation region; and electrical contacts to said gate conductive layer over said contact isolation region.

Claim 16 (withdrawn): The varactor of claim 15 wherein said first and second isolation regions comprise STI structures.

Claim 17 (withdrawn): The method of claim 15 wherein said contact isolation structure comprises a STI structure.

Claim 18 (withdrawn): The method of claim 15 further comprising well contact regions

adjacent to said first and second isolation regions.

Claim 19 (currently amended): A method of forming a semiconductor varactor, comprising:

forming a well region of a first conductivity type in a semiconductor substrate;
forming a gate dielectric layer on said well region;
forming a gate layer on said gate dielectric layer;
forming contact regions of a first conductivity type in said well region of a first conductivity type wherein said contact regions are formed using a source and drain region implantation formation process; and
forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie an isolation region.

Claim 20 (original): The method of claim 19 further comprising forming sidewall structures adjacent to said gate layer.

Claim 21 (original): The method of claim 20 wherein said well region is n-type.

Claim 22 (original): The method of claim 20 wherein said well region is p-type.